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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Cheung	Docket No:	TI-32389.1
Serial No:	10/712,736	Examiner:	Huynh, Kim
Filed:	11/12/2003	Art Unit:	2182

For: METHOD AND DEVICE FOR PROVIDING HIGH DATA RATE FOR A SERIAL PERIPHERAL INTERFACE

APPEAL BRIEF PURSUANT TO 1.192(c)

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at 703-872-9306 on 7-21-05.

Tommie Chambers

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in connection with the above identified application in response to the Final Office Action mailed December 22, 2004, and the Advisory Action mailed March 14, 2005.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1-20 were originally filed, Claim 12 has been cancelled, and Claims 1-6 and 13-20 are withdrawn from consideration. Consequently, the subject matter of the instant appeal is the final rejection of Claims 7-11.

STATUS OF AMENDMENTS

A response filed on August 24, 2004 cancelled Claim 12.

The response After Final Rejection cancelled no claims.

The Advisory Action did not enter the Response After Final Rejection even though no claims were amended.

SUMMARY OF THE CLAIMED SUBJECT MATTER

In accordance with various aspects of the present invention, an improved high performance scheme is provided with a serial peripheral interface (SPI) to enable microcontroller-based products and other components and devices to achieve a higher serial transmit and receive data rate. In accordance with an exemplary embodiment, an exemplary technique utilizes a CPU and an SPI having a circular FIFO structure, configured with a single port memory device. To prevent the memory traffic associated with any SPI accesses from conflicting with other CPU memory accesses, the technique utilizes cycle stealing direct memory access techniques for SPI data transfers with the memory.

In accordance with an exemplary embodiment, during a CPU read/write sequence, data is read/written from/to the memory through a virtual special function register (SFR). Once the virtual SFR access is detected, all accesses are redirected to the circular FIFO buffer memory, with no additional pipelining necessary.

Microcontroller 100 is suitably configured in communication with microcontroller 101 via communication path 150. Microcontroller 100 suitably comprises a central processing unit (CPU) core 102 configured for the processing of data, and a Bus Interface ("BusIF") 104 for communication with the various memory or input and output devices. Microcontroller 100 can include an internal CPU memory 106 which can be implemented using static random access memory (SRAM) and the like which can provide very low access time, e.g., as low as 10 nanoseconds. In addition, microcontroller 100 can also include data memory 114 which can also comprise SRAM-type memory, and read-only memory (ROM) 116 which can comprise the non-reprogrammable memory for the microcontroller 100. Still further, microcontroller 100 can also include flash memory for the programming and storage of data, such as a large page of memory 124 including, for example, 32 KB of data storage, as well as a smaller configuration of flash memory 126, comprising, for example, 128 bytes.

For the transmitting and receiving of data between various components, microprocessor 100 can also include serial peripheral interface (SPI) 108. SPI 108 may communicate directly with CPU core 102 via BusIF 104 or may communicate directly with the CPU memory 106 via direct memory access (DMA) 112 and BusIF 104. In other words, SPI 108 can transfer data to and from memory without passing the data through the CPU. Furthermore, SPI 108 can transmit and receive information from other microcontroller devices. For example, SPI 108 may communicate, over communications path 150, with microprocessor device 101. SPI 108 may be an integral part of a peripheral device or may be a stand alone interface apart from and in communication with the peripheral device.

SPI 108 comprises shift registers for receiving and sending data via communication lines such as: Master In Slave Out and Master Out Slave In lines. SPI 108 may further be configured to operate in either a master or slave mode.

In accordance with an exemplary embodiment, an exemplary technique utilizes a CPU and an SPI having a circular FIFO structure, configured with a single port memory device. To prevent the memory traffic associated with any SPI accesses from conflicting with other CPU memory accesses, the technique utilizes cycle stealing direct memory access techniques for SPI data transfers with the memory. The cycle stealing direct memory access (DMA) techniques may be employed such that the DMA module waits until the CPU is not using the bus interface before the DMA module transfers data between the serial peripheral interface and memory.

GROUNDS OF REJECTION

The sole issue on appeal is whether Claims 7-11 are unpatentable under 35 U.S.C. § 103 as being obvious over Hill in view of Sowell.

ARGUMENTS

It is respectfully submitted that Hill does not disclose or suggest the presently claimed invention including the SPI being further configured to communicate with DMA module and the bus interface for providing cycle stealing.

Applicants agree with the Examiner as evidence by page 4 of the Office Action that Hill does not disclose the SPI for providing cycle stealing.

It is respectfully submitted that Sowell does not disclose or suggest the presently claimed invention including the SPI being further configured to communicate with the DMA module and the bus interface for providing cycle stealing.

The Honorable Board's attention is directed to column 3, lines 5-10 of Sowell.

Here, Sowell discloses that the direct memory access DMA provides a fast means for retrieving and placing data that is required for the HDLC block. The DMA is generally used in a "cycle stealing mode" which provides an efficient means of data movement.

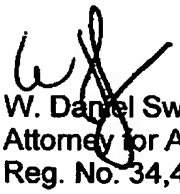
Sowell or any prior art reference applied by the Examiner does not disclose a SPA having cycle stealing.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 7-11 under 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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APPENDIX

Claim 1 (withdrawn): A microcontroller for industrial control comprising:

a central processing unit (CPU);

a bus interface in communication with the CPU;

a CPU memory module in communication with the bus interface; the CPU memory module configured to include a FIFO memory buffer;

a direct memory access module in communication with the bus interface; and

a serial peripheral interface (SPI) module in communication with the direct memory access module and the bus interface; the SPI module having hardware configured to maintain pointers to addresses within the FIFO memory buffer; the SPI module hardware configured to maintain counters; and the SPI module configured to use the FIFO memory buffer, pointers and counters as a transmission buffer for external communications for creating a virtual special function register.

Claim 2 (withdrawn): The microcontroller of claim 1 the SPI module further comprising a transmitter buffer and a receiver buffer; wherein the transmitter buffer is configured to transmit data from the FIFO memory buffer, and wherein the receiver buffer is configured to transmit data to the FIFO memory buffer.

Claim 3 (withdrawn): The microcontroller of claim 1 the SPI module further configured to operate as one of a master device and a slave device.

Claim 4 (withdrawn): The microcontroller of claim 1 the SPI module further configured to provide a data register chip select signal.

Claim 5 (withdrawn): The microcontroller of claim 1 the SPI module further configured to provide at least one of a CPU transmitter pointer signal, a CPU receiver pointer signal, a SPI transmitter pointer signal and a SPI receiver pointer signal.

Claim 6 (withdrawn): The microcontroller of claim 1 the microcontroller further comprising a DMA module configured to communicate with the SPI module and the bus interface for providing cycle stealing.

Claim 7 (previously presented): A serial peripheral interface (SPI) for use with a microcontroller and configured for increasing the rate of data communications, wherein the SPI module comprises:

a plurality of hardware pointers to memory locations in a FIFO buffer;

at least one hardware pointer counter; and

a hardware logic device; wherein the hardware logic device is configured to communicate with a bus interface and to utilize the FIFO buffer for intermediate storage of data being transmitted from and received to the CPU,

wherein the SPI is further configured to communicate with a DMA module and the bus interface for providing cycle stealing.

Claim 8 (original): The SPI of claim 7 wherein the plurality of hardware pointers are configured to provide at least one of a CPU transmitter pointer signal, a CPU receiver pointer signal, a SPI transmitter pointer signal and a SPI receiver pointer signal.

Claim 9 (original): The SPI of claim 7 the SPI module further comprising a transmitter buffer and a receiver buffer; wherein the transmitter buffer is configured to transmit data from the FIFO buffer, and wherein the receiver buffer is configured to transmit data to the FIFO buffer.

Claim 10 (original): The SPI of claim 7 the SPI module further configured to operate as one of a master device and a slave device.

Claim 11 (original): The SPI of claim 7 the SPI module further configured to provide a data register chip select signal to the bus interface.

Claim 12 (cancelled).

Claim 13 (withdrawn): A method for increasing a microprocessor data communication rate through a serial peripheral interface (SPI) module comprising the steps of:

a) storing a first value from a Central Processing Unit (CPU) to a virtual special function register (SFR);

b) retrieving the first value from the virtual SFR and transmitting the first value through a Serial Peripheral Interface (SPI) module;

c) receiving a second signal at the SPI module and storing the second signal in the virtual SFR; and

d) communicating the second signal from the virtual SFR to the CPU;

wherein the virtual SFR comprises memory addresses within a circular FIFO buffer; and wherein the memory addresses within the circular FIFO buffer are identified by hardware pointers in the SPI module.

Claim 14 (withdrawn): The method of claim 13 further comprising the step of using cycle stealing techniques; wherein a DMA module is configured to communicate with the bus interface and SPI module.

Claim 15 (withdrawn): The method of claim 14 wherein the step of storing the first value further comprises the steps of:

providing a write signal, a virtual SFR address signal, and a data signal from the CPU to the SPI module;

sending, to a bus interface from the SPI module, a DRCS signal, and a CPU transmitter pointer address signal; and

writing from the bus interface to a FIFO memory device at an address indicated by the transmitter pointer address signal.

Claim 16 (withdrawn): The method of claim 14 wherein the step of retrieving the first value further comprises the steps of:

detecting the presence of data to be sent on the FIFO buffer;

sending a SPI transfer request signal and a SPI transfer pointer signal to a DMA module;

requesting, by the DMA module, bus interface time and providing a DMA address signal and a DMA read signal to the bus interface;

reading a first value from the DMA address in the FIFO memory buffer to the bus interface;

providing the first value from the bus interface to the DMA module, and providing the first value from the DMA module to the SPI module; and

transmitting the data via a transmit shift register and transmit buffer.

Claim 17 (withdrawn): The method of claim 16 wherein the step of retrieving the first value further comprises the steps of:

receiving an acknowledgement from the bus interface at the DMA module indicating that the FIFO memory has been read; and

providing the acknowledgement to the serial peripheral interface module.

Claim 18 (withdrawn): The method of claim 14 wherein the step of receiving and storing the second value further comprises the steps of:

sending the second value received at the SPI module to a DMA module;

sending a SPI receive request signal and a SPI receive pointer signal to a DMA module;

sending a DMA request signal, DMA write signal, DMA address signal and DMA data signal to the Bus interface; and

writing the DMA data signal to the FIFO buffer, and keeping track of the storage location by use of pointers in the serial peripheral interface;

Claim 19 (withdrawn): The method of claim 14 wherein the step of receiving and storing the second value further comprises the steps of:

receiving an acknowledgement at the DMA indicating the second value was written to the FIFO buffer; and

sending the acknowledgement from the DMA module to the SPI module.

Claim 20 (withdrawn): The method of claim 14 wherein the step of communicating the second value further comprises the steps of:

receiving, at a bus interface and SPI module, a read command signal and virtual SFR address signal from the CPU;

sending a data register chip select signal and FIFO pointer address to the bus interface; wherein the FIFO memory address is the address indicated by a pointer stored in the SPI module; and

reading the second value from that memory location to the CPU.

EVIDENCE APPENDIX

Appellants are submitting no items of evidence.

RELATED PROCEEDINGS APPENDIX

Appellants have no submission for the Related Proceeding Appendix.

